

Charge-Trapping Memory Cell Array and Method for Production

ABSTRACT OF THE DISCLOSURE

In a memory cell array comprising charge-trapping memory cells, local interconnects along the direction of the wordlines for connecting source/drain regions of adjacent memory cells to bitlines are formed by selective deposition of silicon or polysilicon bridges at sidewalls of the semiconductor material within upper recesses in the dielectric material of shallow trench isolations running across the wordlines.